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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/652,028	09/02/2003	Takahiro Fujioka	HITA.0426	1544

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EXAMINER	
KUMAR, SRILAKSHMI K	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/652,028	FUJIOKA ET AL.	
	Examiner	Art Unit	
	Srilakshmi K. Kumar	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The following office action is in response to the after final amendment filed on March 2, 2007.

Claims 11-15 are pending. The finality of the previous office action has been withdrawn.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 11-15 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 5 of U.S. Patent No. 6,862,015. Although the conflicting claims are not identical, they are not patentably distinct from each other because

	Instant application 10/652028		Patented Case 6,862,015
Claim 11:	A liquid crystal display device comprising: a liquid	Claim 9:	A liquid crystal display device having a liquid crystal display

	crystal display panel; a first liquid crystal drive circuit and a second liquid crystal drive circuit; a first image signal line and a first clock signal line formed on the liquid crystal display panel, and connected with the first liquid crystal drive circuit; and a second image signal line and a second clock signal line formed on the liquid crystal display panel, and connected with the first liquid crystal drive circuit and the second liquid crystal drive circuit, wherein the first liquid crystal drive circuit comprises a first image signal input terminal connected with the first image signal line, and a first clock input terminal		element, a plurality of cascade-connected liquid crystal drive circuits, and a plurality of signal lines formed over an edge portion of the liquid crystal display element for transmitting a signal between any two of the drive circuits, wherein each of the liquid crystal drive circuits comprises: a data input terminal connected with one of the signal lines to receive an external image signal being input thereto as an internal image signal into said each of the liquid crystal drive circuits;

	connected with the first clock signal line, and the second liquid crystal drive circuit comprises a second image signal input terminal connected with the second image signal line and a second clock input terminal connected with the second clock signal line; wherein the first liquid crystal drive circuit comprises a compensation circuit configured to generate an internal clock signal based on a clock received from the first clock input terminal signal compensating for a duty ratio deviation of the received clock signal, the internal clock signal swinging from a first voltage to a second		a clock compensation circuit for inputting an external clock signal and outputting an internal clock signal, the internal clock signal having a first period for outputting a first voltage and a second period for outputting a second voltage;

	voltage lower than the first voltage, a data select circuit configured to select digital image data received from the first image signal input terminal at a timing of a voltage change from the first voltage to the second voltage as a first digital image data and at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal as a second digital image data; a first data bus configured to transmit the first digital image data from the data select circuit, a second data bus configured to transmit the second digital image data from the data		a first data latch circuit for taking thereto the internal image signal at a timing of a voltage change from the first voltage to the second voltage of the internal cloak as a first image signal; a second data latch circuit for taking thereto the internal image signal at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal of the internal cloak as a second image signal; a first data bus for transmitting the first image signal from the first data latch circuit; a second data bus for transmitting the second image signal from the second data latch circuit;

	select circuit, a select voltage circuit configured to select a voltage according with the first and the second digital image data to drive the liquid display panel, a image signal output circuit configured to output the digital image data received from the first image signal input terminal to the second liquid crystal drive circuit via the second image signal line, and a clock signal output circuit configured to delay the internal clock signal and output the delayed clock signal to the second liquid crystal drive circuit via the		a voltage output circuit for outputting a voltage selected according with the first and the second image signals on the first and second data buses to the liquid crystal display element; a data output circuit for outputting the image signal on the data bus to a subsequent liquid crystal drive circuit; a clock formation circuit being operable to correct a duty ratio deviation of the external clock signal to provide the internal clock signal; and a clock signal output circuit for outputting the internal clock signal as a subsequent external clock signal and for outputting the first image signal and the second image signal in sequence as a subsequent

	second clock signal line.		external image signal to a subsequent liquid crystal drive circuit, said clock signal output circuit having a delay circuit, wherein the internal clock signal is delayed to become the subsequent external clock signal by the delay circuit so as to provide phase margins thereof in a dual-edge accept scheme.

The instant application teaches a first and second circuit which would be the same as a plurality of circuits as taught by the patented case. The first image signal input terminal and second image signal input terminal corresponds to the data input terminal of the patented case. The data select circuit of the instant application corresponds to the data latch circuits of the patented case, as the applicant has pointed out in the after final response to the instant application. As shown from the side-by-side comparison, the instant application and the patented case claim the similar subject matter, where the patented case teaches narrower subject matter.

Dependent claims 12-15 are similarly rejected under obvious type double patenting.

Response to Arguments

3. Applicant's arguments with respect to claims 11-15 have been considered but are moot in view of the new ground(s) of rejection.

With applicant's clarification of the limitation of " a data select circuit configured to select digital image data received from the first image signal input terminal...as a second digital image data", the 35 USC 112, first paragraph, rejection has been withdrawn. A double patenting rejection has been issued as shown above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srilakshmi K. Kumar whose telephone number is 571 272 7769. The examiner can normally be reached on 9:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571 272 3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Srilakshmi K. Kumar
Examiner
Art Unit 2629

SKK
March 26, 2007

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER